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What is claimed is:

- 1 1. An apparatus, comprising:
  - 2 a request queue coupled to a memory unit via a memory-sensing device;
  - 3 a response queue coupled to the memory-sensing device; and
  - 4 an arbiter coupled to said response queue.
- 1 2. The apparatus of claim 1, wherein the memory-sensing device comprises redundant circuitry capable of sensing memory in the memory unit substantially simultaneously.
- 1 3. The apparatus of claim 1, wherein said request queue comprises memory to store more than one request.
- 1 4. The apparatus of claim 3, wherein the memory to store more than one request comprises memory to service more than one request substantially simultaneously.
- 1 5. The apparatus of claim 1, wherein said response queue comprises memory to store data for a response.
- 1 6. The apparatus of claim 1, wherein said arbiter comprises a response arbiter to determine a response to more than one request.
- 1 7. The apparatus of claim 6, wherein the response arbiter comprises a priority determiner to determine a priority of a response to a request.
- 1 8. The apparatus of claim 1, wherein said arbiter comprises a request arbiter coupled to said request queue.

1    9.    A method, comprising:

2        receiving more than one request for sensing data in a memory unit;

3        sensing data in the memory unit;

4        returning critical data in response to said receiving more than one request; and

5        returning non-critical data.

1    10.   The method of claim 9 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a second transaction before completing a response to a first transaction.

1    11.   The method of claim 9 wherein said receiving more than one request for sensing data in a memory unit comprises receiving a request to read critical data.

1    12.   The method of claim 9 wherein said sensing data in the memory unit comprises determining an order to sense data based on available redundant circuitry.

1    13.   The method of claim 9 wherein said returning critical data comprises interrupting a response to a first request comprising non-critical data to return critical data in response to a second request.

1    14.   The method of claim 9 wherein said returning non-critical data comprises returning non-critical data in accordance with a pre-defined protocol.

1    15.   The method of claim 14 wherein returning non-critical data in accordance with a pre-defined protocol comprises responding to each request of the more than one request with time-sliced burst data.

1    16.   The method of claim 14 wherein returning non-critical data in accordance with a pre-defined protocol comprises returning non-critical data in an order based upon a priority attached to the more than one request.

1 17. A system, comprising:

2           a virtual-port memory device;  
3           a memory controller coupled to said virtual-port memory device; and  
4           a host coupled to said memory controller.

1 18. The system of claim 17, wherein said virtual-port memory device comprises:

2           a request queue coupled to a memory unit via a memory sensing device;  
3           a response queue coupled to the memory sensing device; and  
4           an arbiter coupled to said response queue.

1 19. The system of claim 18, wherein the arbiter comprises a response arbiter to determine  
2           a response to more than one request.

1 20. The system of claim 17, wherein said memory controller comprises:

2           a response interpreter coupled to said virtual-port memory device;  
3           a host response queue coupled to the response interpreter; and  
4           a host request queue coupled to said host.

1 21. A system, comprising:  
2           a virtual-port memory device coupled to a microprocessor; and  
3           an input-output device coupled to the microprocessor.

1 22. The system of claim 21, wherein said virtual-port memory device comprises:  
2           a request queue coupled to a memory unit via a memory sensing device;  
3           a response queue coupled to the memory sensing device; and  
4           an arbiter coupled to said response queue.

1 23. The system of claim 21, wherein said input-output device comprises an antenna  
2           device.

1 24. The system of claim 21, wherein said input-output device comprises an audio input  
2           device and an audio output device.

- 1    25. A machine-readable medium containing instructions, which when executed by a  
2    machine, cause said machine to perform operations, comprising:  
3         receiving more than one request for sensing data in a memory unit;  
4         sensing data in the memory unit;  
5         returning critical data in response to said receiving more than one request; and  
6         returning non-critical data.
- 1    26. The machine-readable medium of claim 25 wherein said receiving more than one  
2    request for sensing data in a memory unit comprises receiving a second transaction  
3    before completing a response to a first transaction.
- 1    27. The machine-readable medium of claim 25 wherein said receiving more than one  
2    request for sensing data in a memory unit comprises receiving a request to read  
3    critical data.
- 1    28. The machine-readable medium of claim 25 wherein said sensing data in the memory  
2    unit comprises determining an order to sense data based on available redundant  
3    circuitry.
- 1    29. The machine-readable medium of claim 25 wherein said returning critical data  
2    comprises interrupting a response to a first request comprising non-critical data to  
3    return critical data in response to a second request.
- 1    30. The method of claim 25 wherein said returning non-critical comprises returning non-  
2    critical data in accordance with a pre-defined protocol.

1 31. An apparatus, comprising:  
2       a memory unit;  
3       a memory-sensing device coupled with said memory unit;  
4       a request queue coupled with said memory sensing device to receive more  
5           than one request to sense data in said memory unit; and  
6       an arbiter coupled with said memory sensing device to determine the sequence  
7           to return the data in response to the more than one request.

1 32. The apparatus of claim 31, further comprising a response queue coupled with said  
2       memory sensing device to store the data.

1 33. The apparatus of claim 31, wherein said memory unit comprises a first partition and a  
2       second partition; and said memory-sensing device comprises redundant circuitry  
3       coupled with said memory unit to sense data in the first partition and the second  
4       partition substantially simultaneously.

1 34. The apparatus of claim 31, wherein said request queue comprises memory to store the  
2       more than one request.

1 35. The apparatus of claim 31, wherein said arbiter comprises a response arbiter coupled  
2       with said memory sensing device to determine a response to the more than one  
3       request.

1 36. The apparatus of claim 35, wherein the response arbiter comprises a priority  
2       determiner to determine a priority of the response to the more than one request.

1 37. The apparatus of claim 31, wherein said arbiter comprises a request arbiter coupled  
2       with said request queue to determine a priority to sense data in response to the more  
3       than one request.

1    38. A system, comprising:

2                a memory unit;

3                a memory-sensing device coupled with said memory unit;

4                a request queue coupled with said memory sensing device to receive more

5                than one request to sense data in said memory unit; and

6                an arbiter coupled with said memory sensing device to determine the sequence

7                to return the data in response to the more than one request; and

8                a processor coupled with said request queue to initiate a first request of the

9                more than one request.

1    39. The system of claim 38, further comprising a memory controller coupled between

2                said request queue and said processor.

1    40. The system of claim 38, further comprising an input-output device.